Figure 1

Figure 2

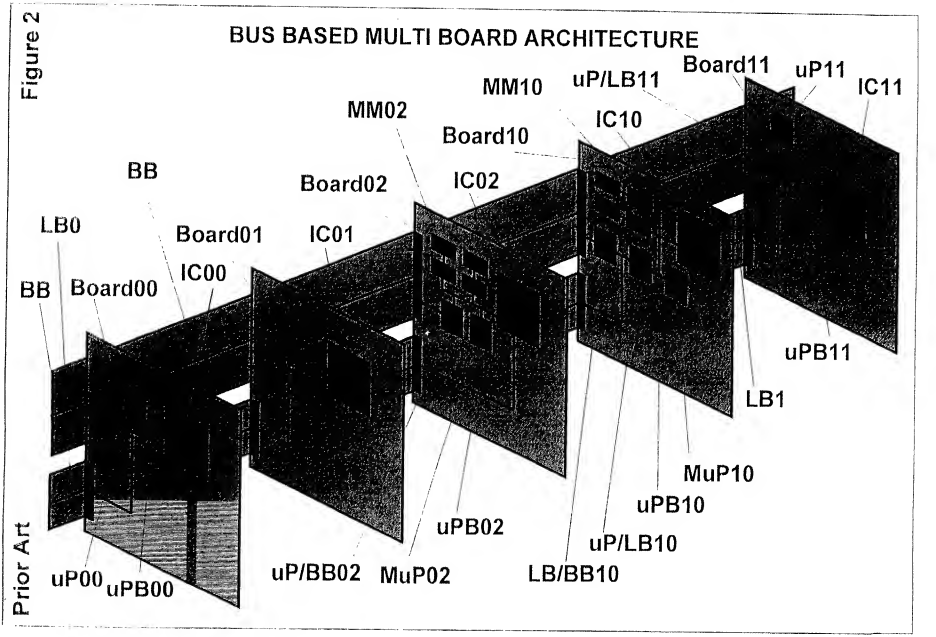
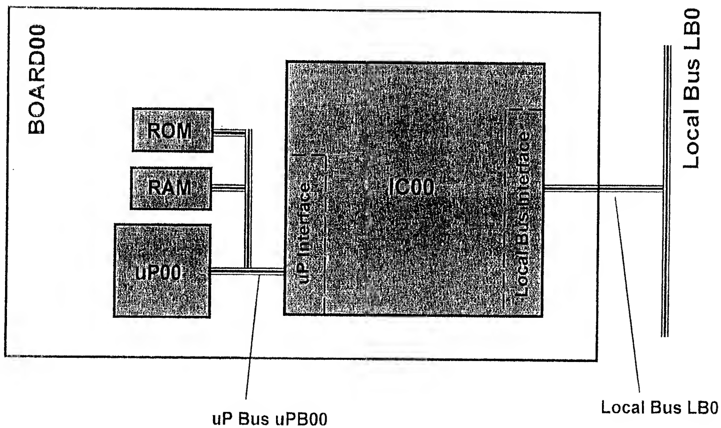


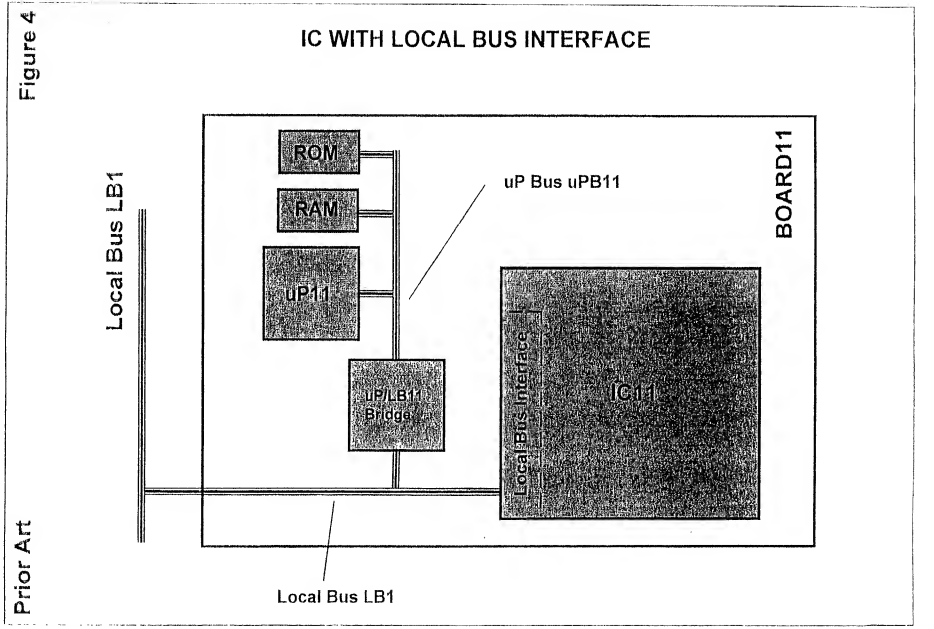
Figure 3

IC WITH uP INTERFACE AND LOCAL BUS INTERFACE



Prior Art

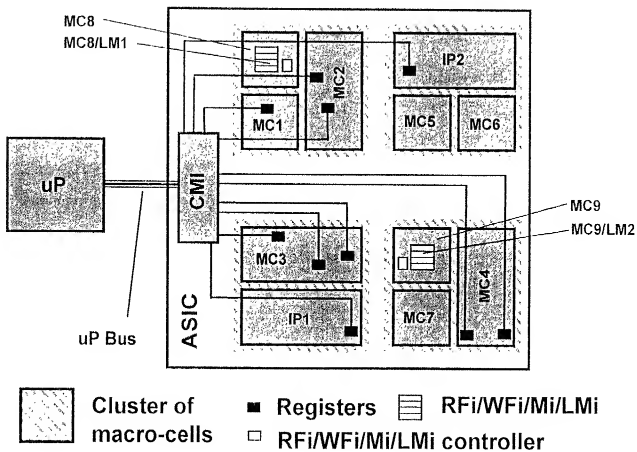
Figure 4



Prior Art

Figure 5

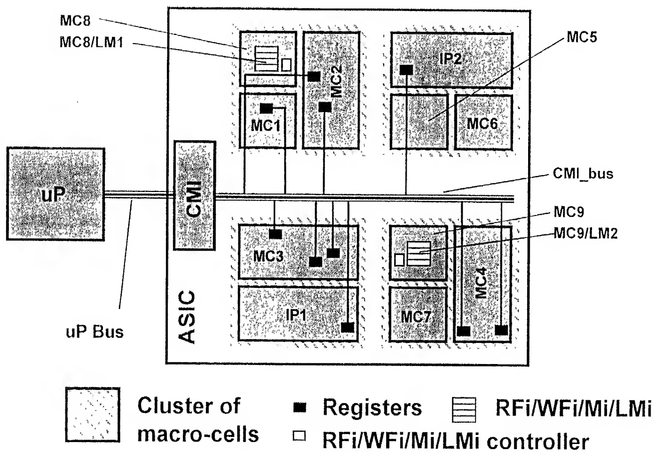
ASIC implementation of CMI with
CMPI macro-cells interface



Prior Art

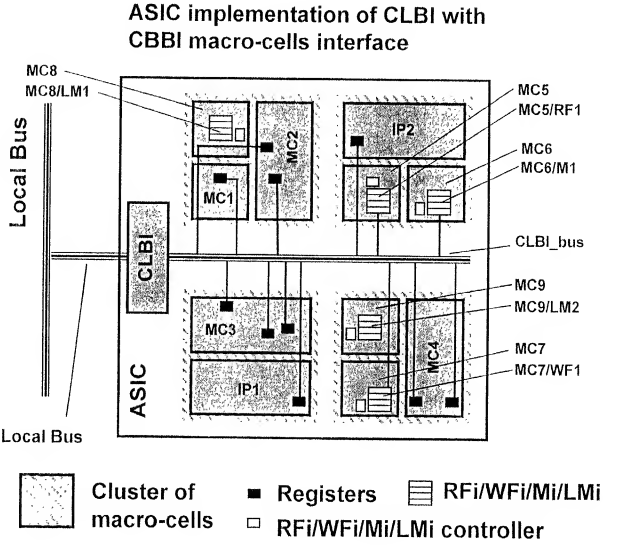
Figure 6

ASIC implementation of CMI with CBBI macro-cells interface



Prior Art

Figure 7



Prior Art

Figure 8

Prior Art

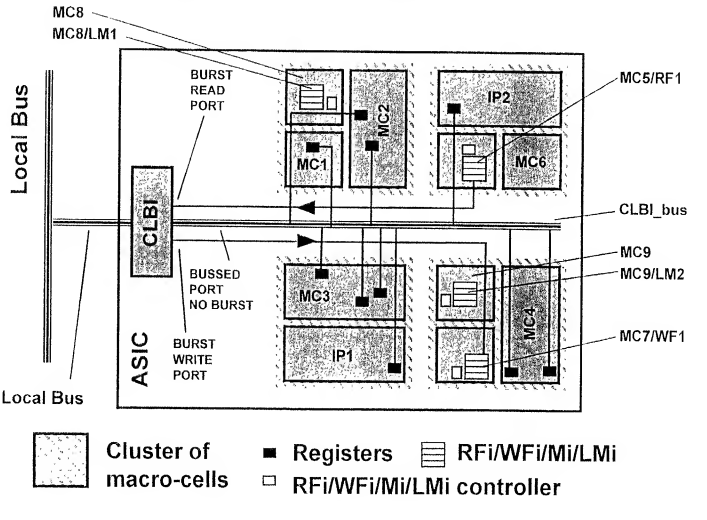


Figure 9

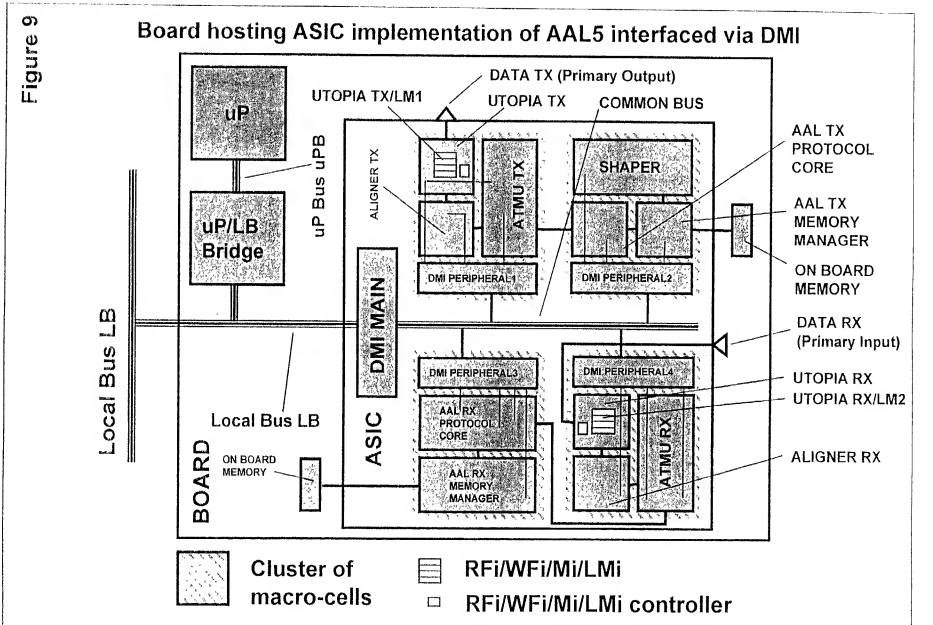


Figure 10

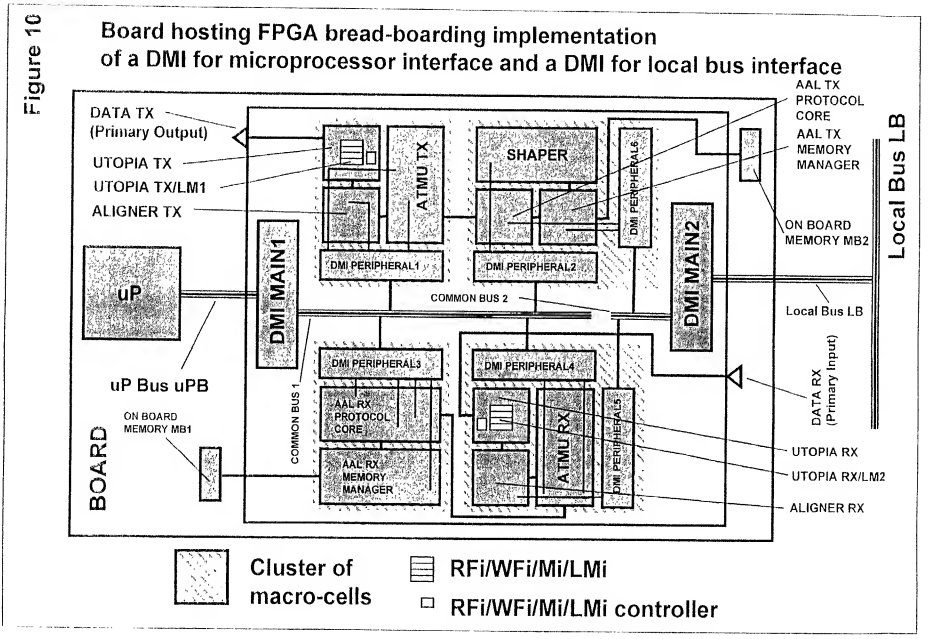


Figure 11

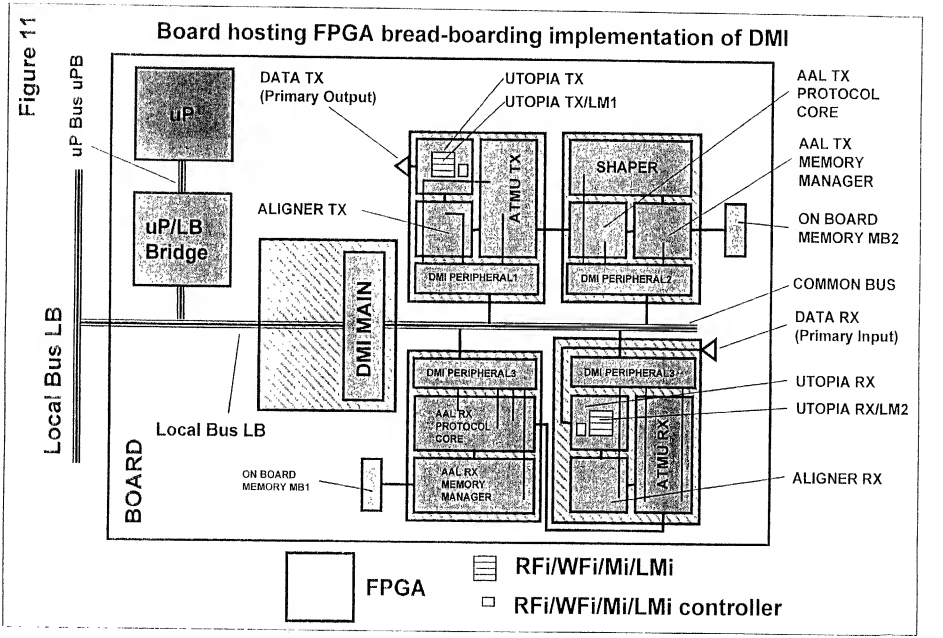


Figure 12

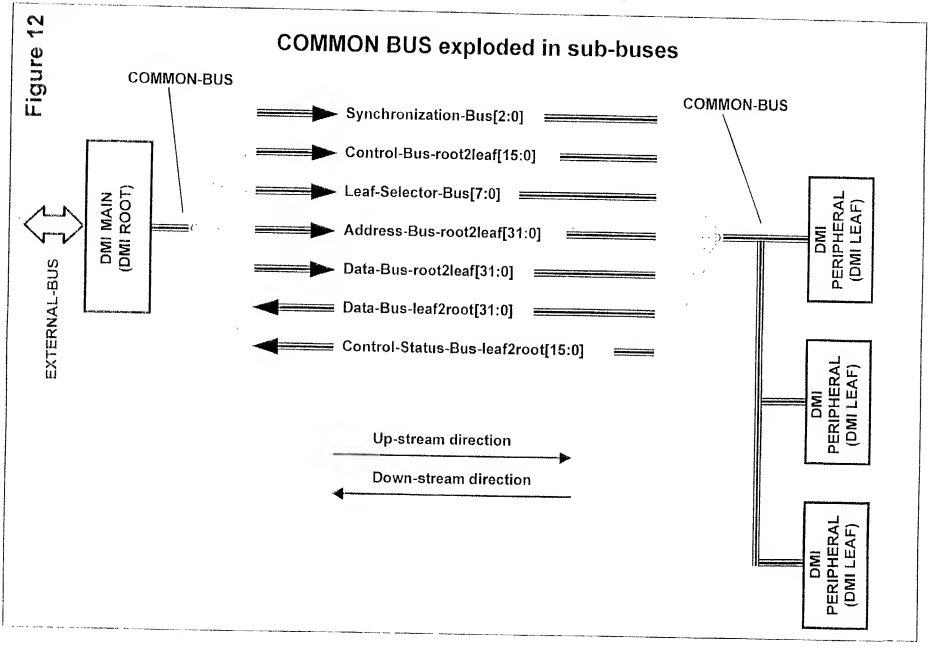


Figure 13

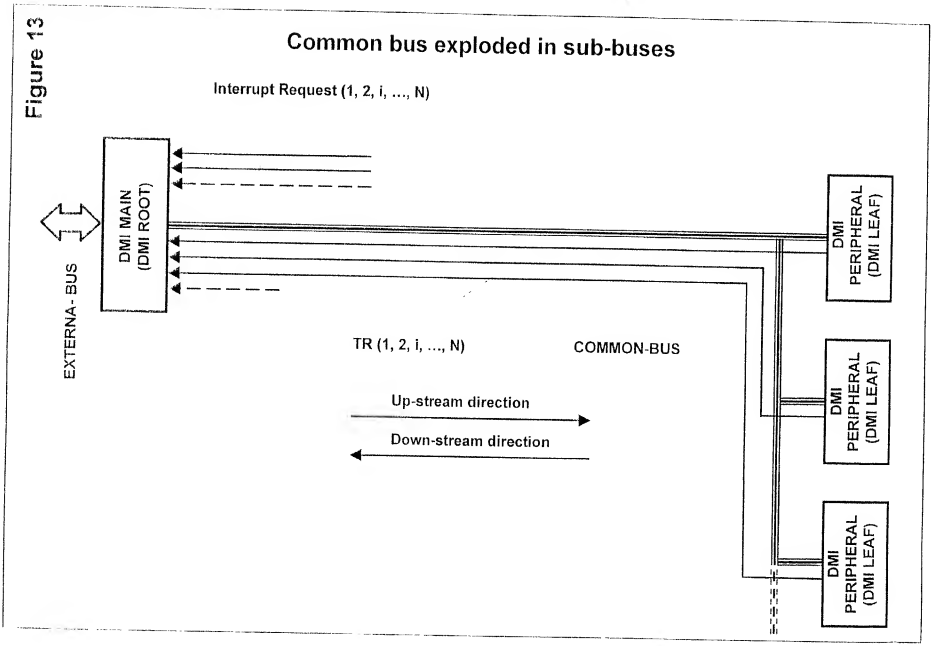


Figure 14

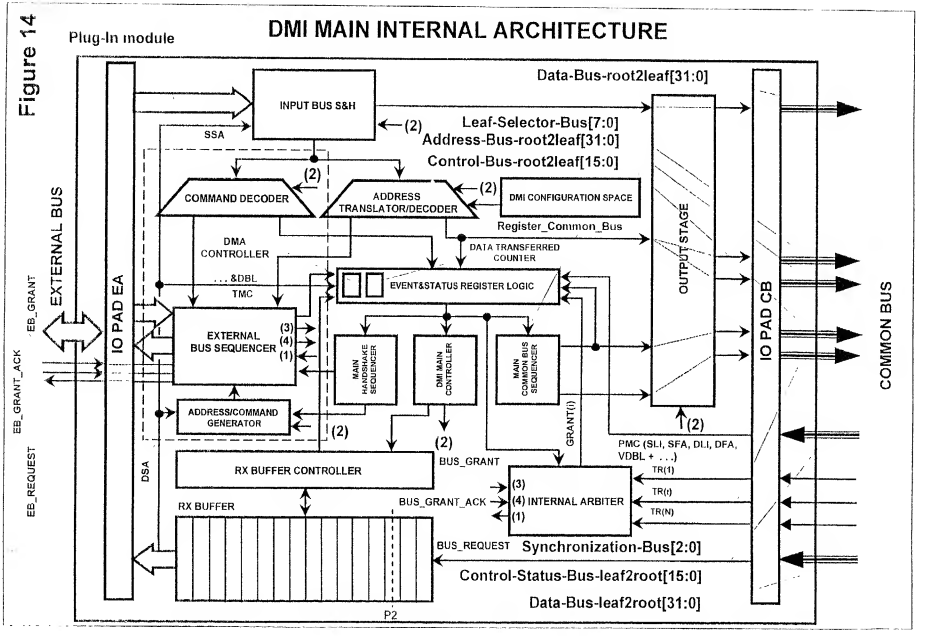


Figure 15

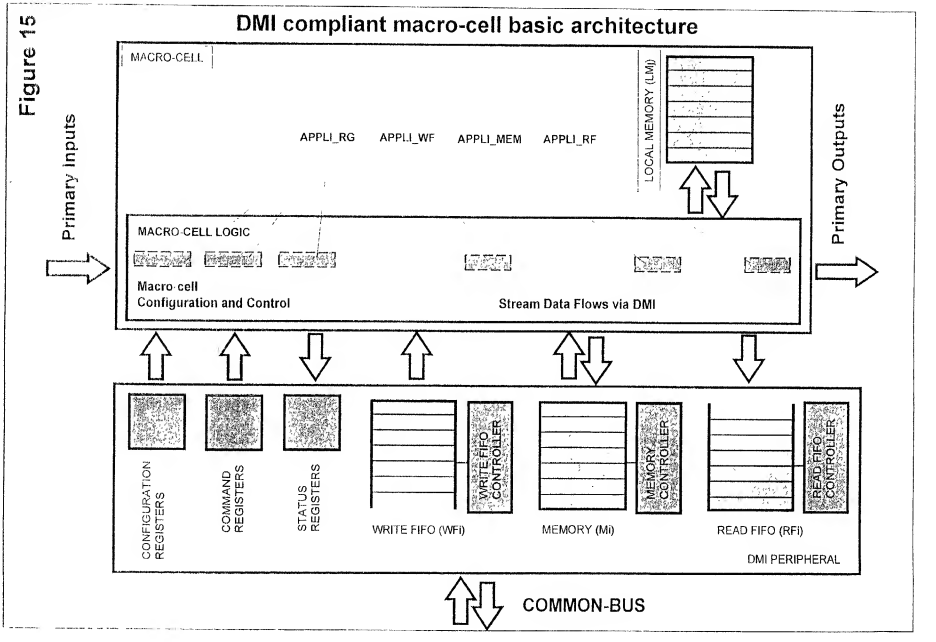
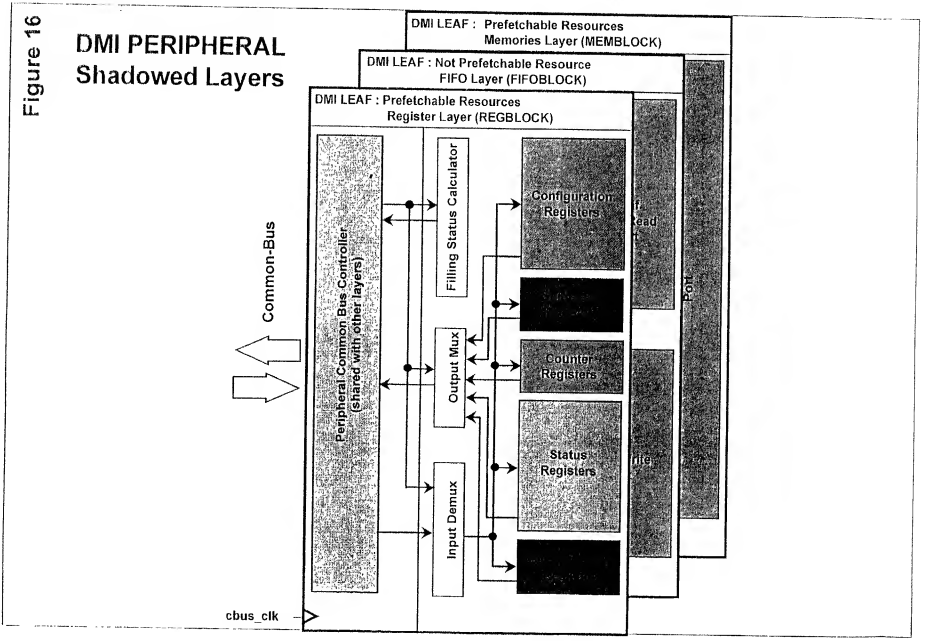


Figure 16



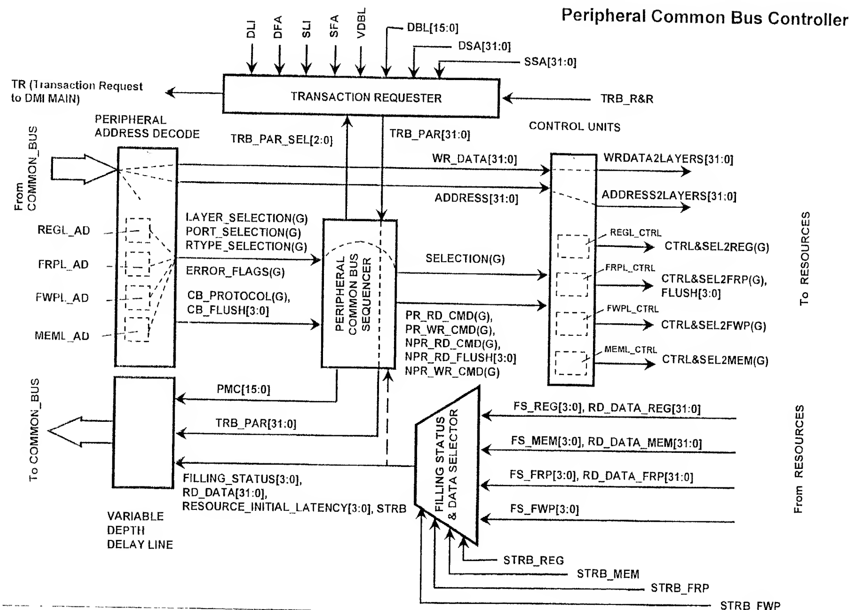

Peripheral Common Bus Controller
DLI
DFA
SLI
SFA
VDBL
DBL[15:0]
DSA[31:0]
SSA[31:0]
TR (Transaction Request to DMI MAIN)
TRANSACTION REQUESTER
TRB_R&R
PERIPHERAL ADDRESS DECODE
TRB_PAR_SEL[2:0]
TRB_PAR[31:0]
CONTROL UNITS
From COMMON_BUS
WR_DATA[31:0]
WRDATA2LAYERS[31:0]
ADDRESS[31:0]
ADDRESS2LAYERS[31:0]
REGL_AD
FRPL_AD
FWPL_AD
MEML_AD
LAYER_SELECTION(G)
PORT_SELECTION(G)
RTYPE_SELECTION(G)
ERROR_FLAGS(G)
CB_PROTOCOL(G),
CB_FLUSH[3:0]
PERIPHERAL COMMON BUS SEQUENCER
SELECTION(G)
PR_RD_CMD(G),
PR_WR_CMD(G),
NPR_RD_CMD(G),
NPR_RD_FLUSH[3:0]
NPR_WR_CMD(G)
REGL_CTRL
CTRL&SEL2REG(G)
FRPL_CTRL
CTRL&SEL2FRP(G),
FLUSH[3:0]
FWPL_CTRL
CTRL&SEL2FWP(G)
MEML_CTRL
CTRL&SEL2MEM(G)
To RESOURCES
To COMMON_BUS
PMC[15:0]
TRB_PAR[31:0]
FILLING_STATUS[3:0],
RD_DATA[31:0],
RESOURCE_INITIAL_LATENCY[3:0], STRB
VARIABLE DEPTH DELAY LINE
FILLING STATUS & DATA SELECTOR
FS_REG[3:0], RD_DATA_REG[31:0]
FS_MEM[3:0], RD_DATA_MEM[31:0]
FS_FRP[3:0], RD_DATA_FRP[31:0]
FS_FWP[3:0]
From RESOURCES
STRB_REG
STRB_MEM
STRB_FRP
STRB_FWP

Figure 17

Figure 18

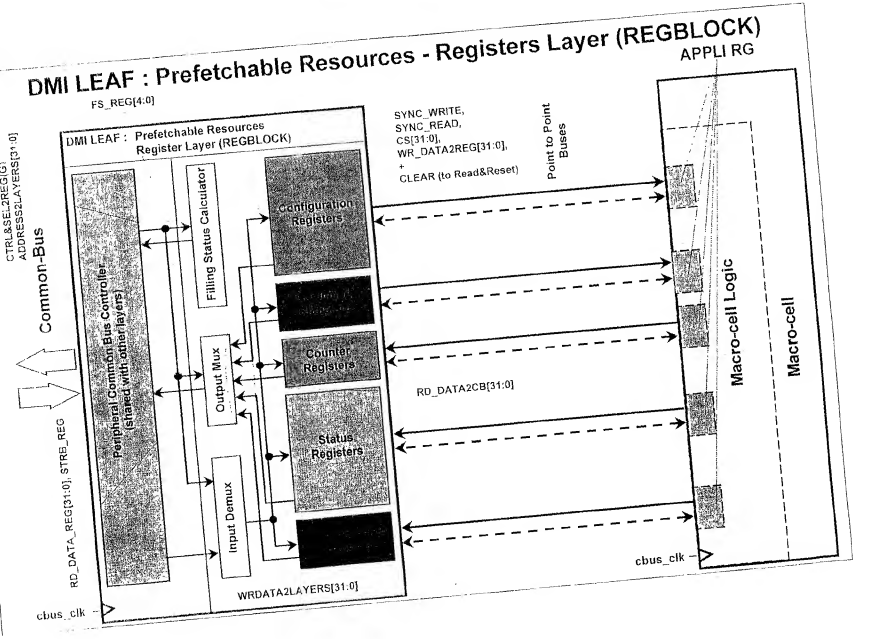
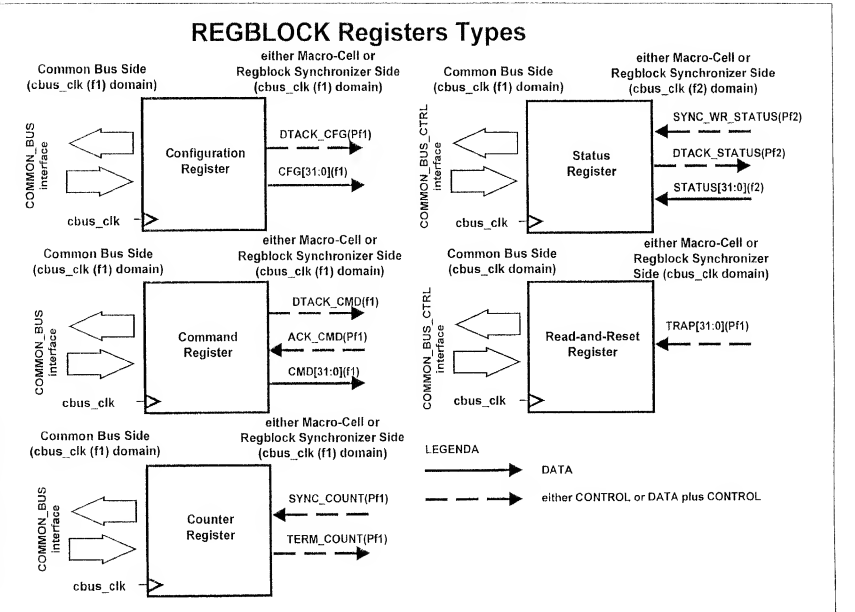


Figure 19

Figure 20



NOTE referred to Counter Register:
DATA_FROM_CB[31:0] is THRESHOLD[31:0]
DATA2CB[31:0] is COUNTER[31:0]

Figure 21

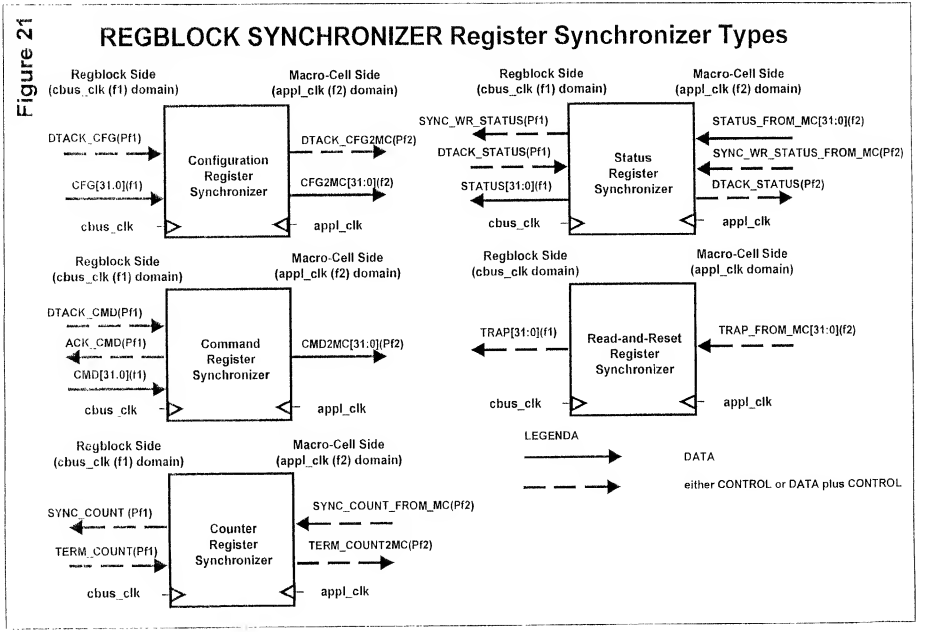


Figure 22

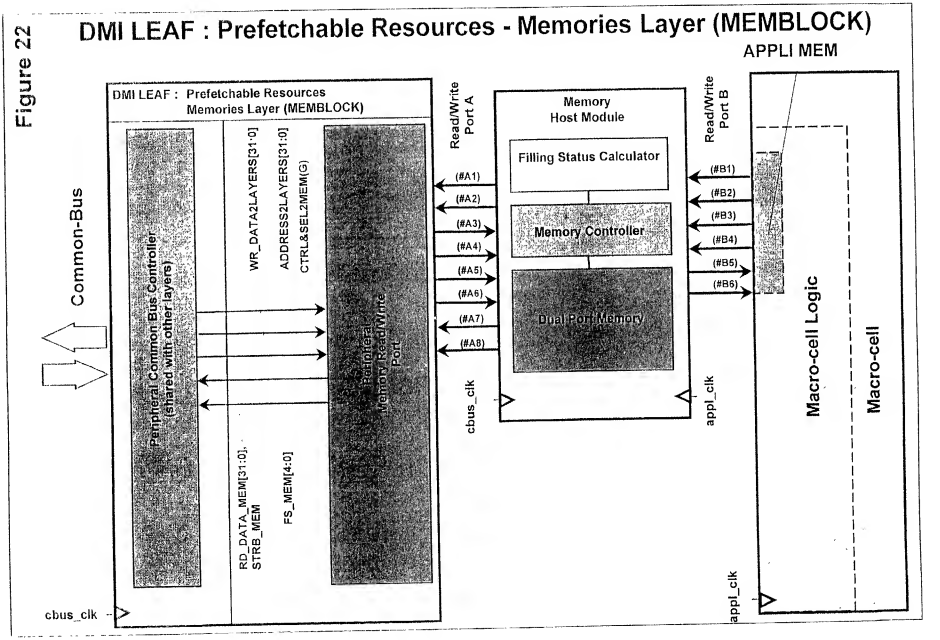

DMI LEAF : Prefetchable Resources - Memories Layer (MEMBLOCK)
APPLI MEM
DMI LEAF : Prefetchable Resources
Memories Layer (MEMBLOCK)
Common-Bus
Peripheral Common Bus Controller
(Shared with other layers)
WR_DATA2LAYERS[31:0]
ADDRESS2LAYERS[31:0]
CTRL&SEL2MEM(G)
Peripheral
Memory Read/Write
Port
RD_DATA_MEM[31:0]
STRB_MEM
FS_MEM[4:0]
cbus_clk
Read/Write
Port A
Memory
Host Module
Filling Status Calculator
Memory Controller
Dual Port Memory
(#A1)
(#A2)
(#A3)
(#A4)
(#A5)
(#A6)
(#A7)
(#A8)
cbus_clk
Read/Write
Port B
(#B1)
(#B2)
(#B3)
(#B4)
(#B5)
(#B6)
appl_clk
Macro-cell Logic
Macro-cell
appl_clk

Figure 23

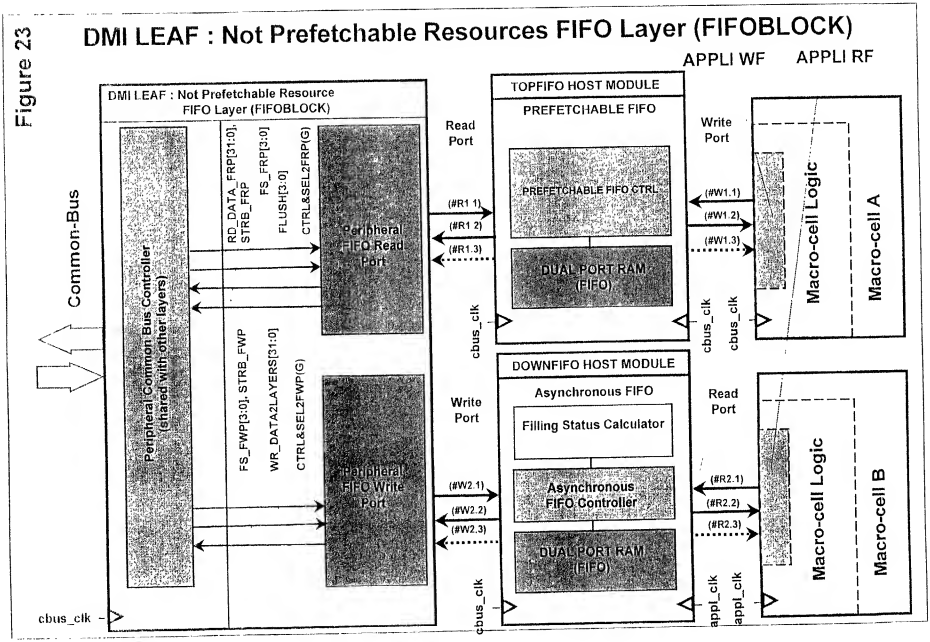
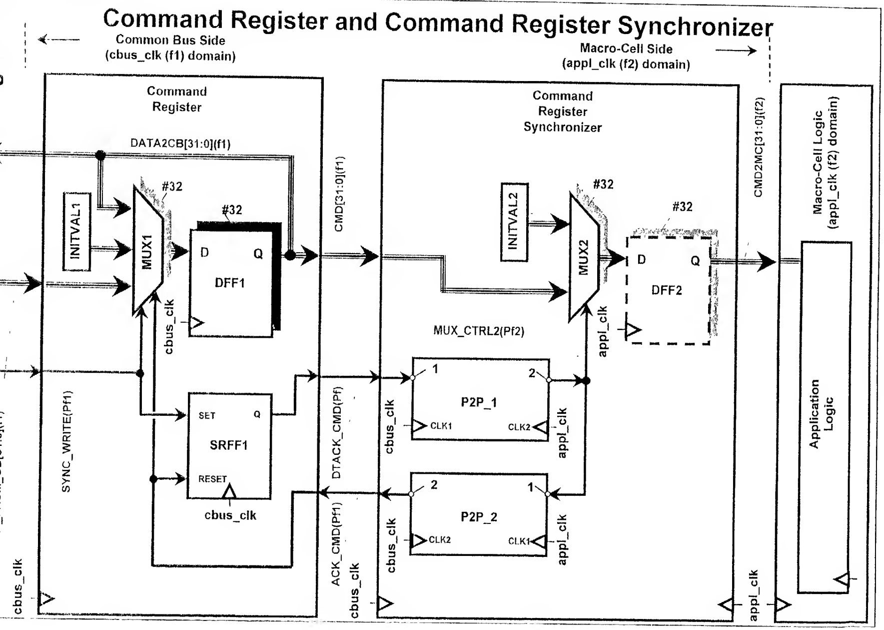


Figure 24



Command Register and Command Register Synchronizer
Common Bus Side
(cbus_clk (f1) domain)
Macro-Cell Side
(appl_clk (f2) domain)
Command
Register
DATA2CB[31:0](f1)
INITVAL1
MUX1
#32
DFF1
D
Q
cbus_clk
SRFF1
SET
RESET
DATA_FROM_CB[31:0](f1)
SYNC_WRITE(Pf1)
CMD[31:0](f1)
DTACK_CMD(Pf)
ACK_CMD(Pf1)
Command
Register
Synchronizer
INITVAL2
MUX2
DFF2
MUX_CTRL2(Pf2)
P2P_1
P2P_2
CLK1
CLK2
appl_clk
CMD2MC[31:0](f2)
Macro-Cell Logic
(appl_clk (f2) domain)
Application
Logic

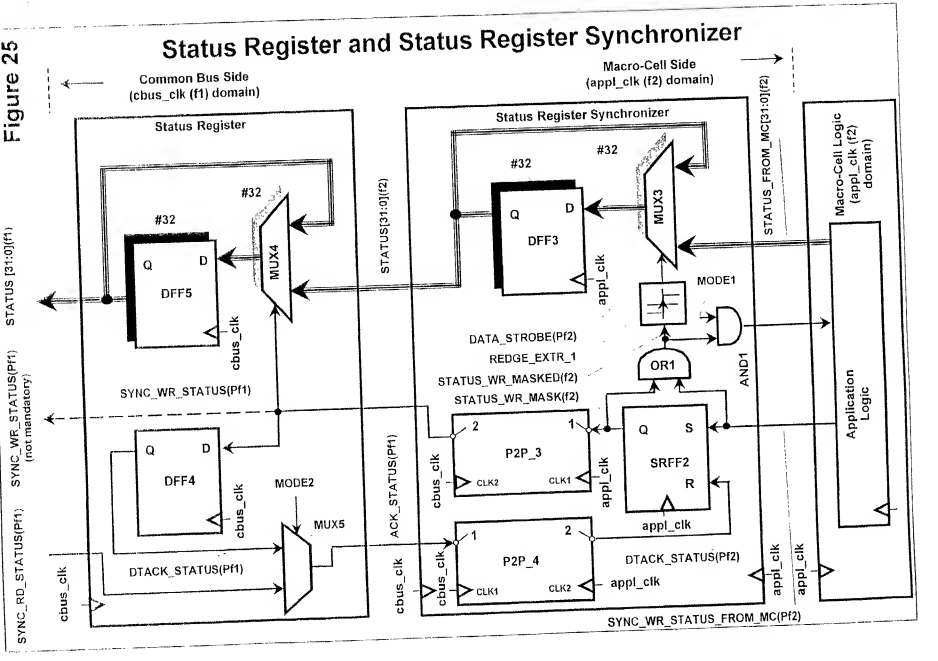


Figure 25

Figure 26

Pulse to Pulse Synchronization Unit

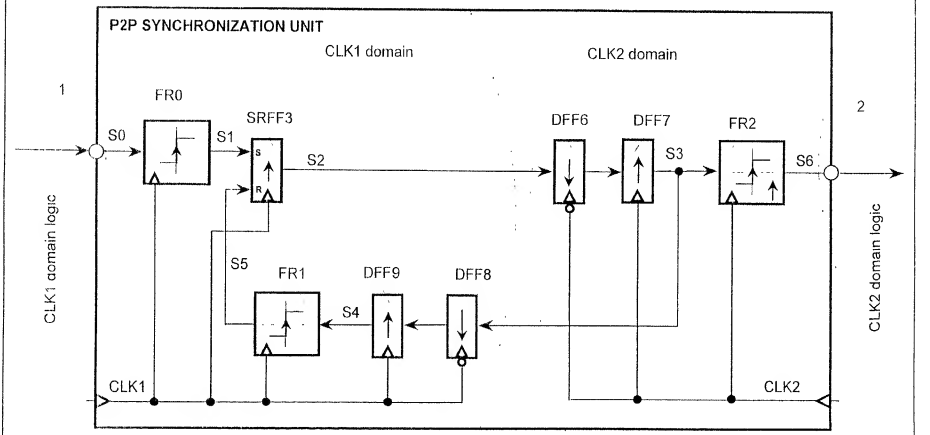


Figure 27

Timing Diagram of Pulse to Pulse Synchronization Unit

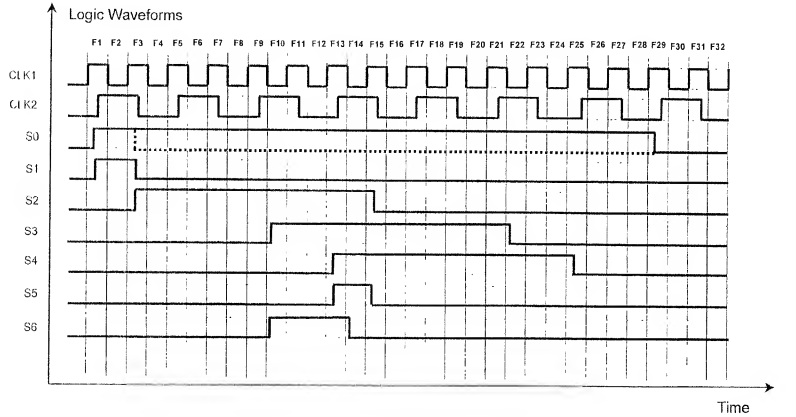


Figure 28

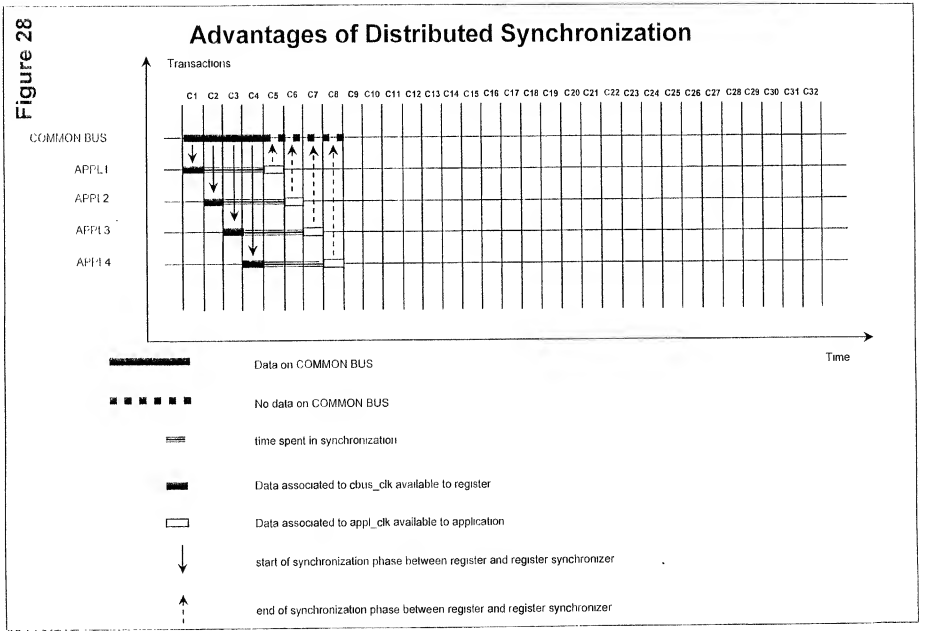


Figure29

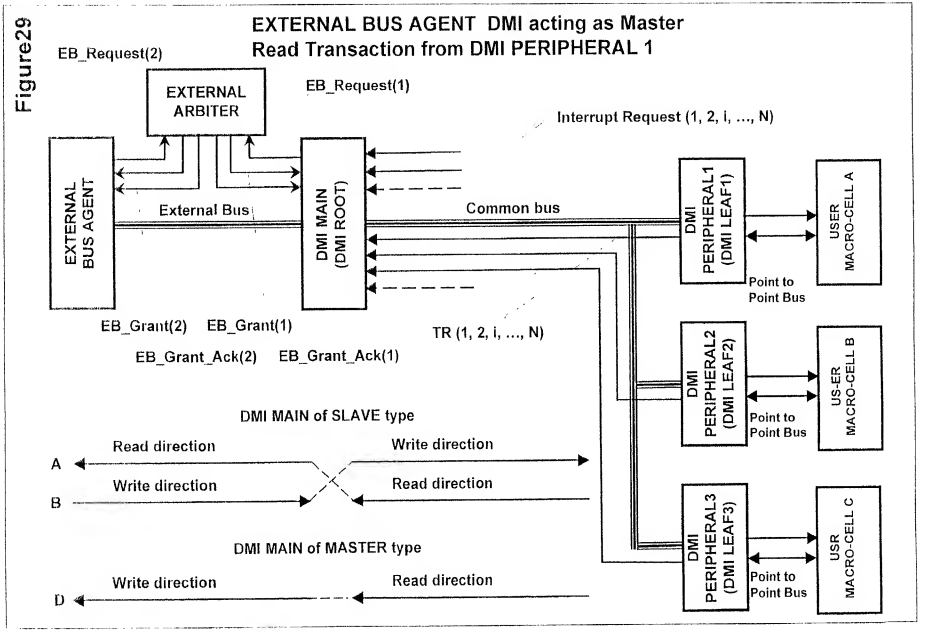
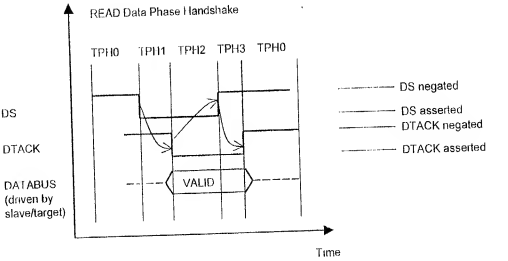


Figure 30

Asynchronous two phase handshake protocol: read



Prior Art

Figure 31

Prior Art

Asynchronous two phase handshake protocol: write

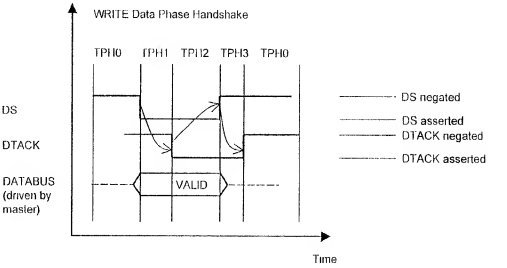
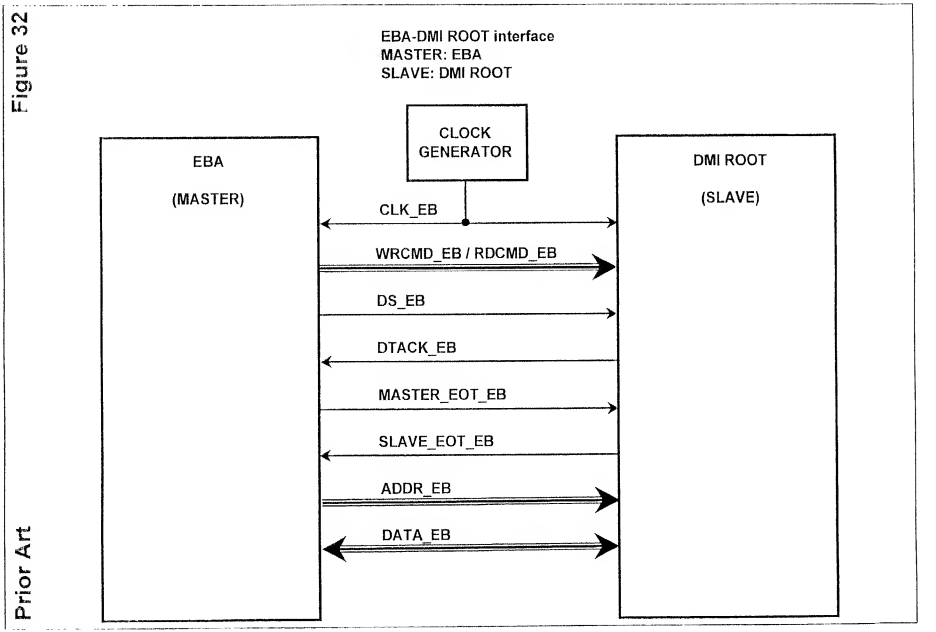


Figure 32



Prior Art

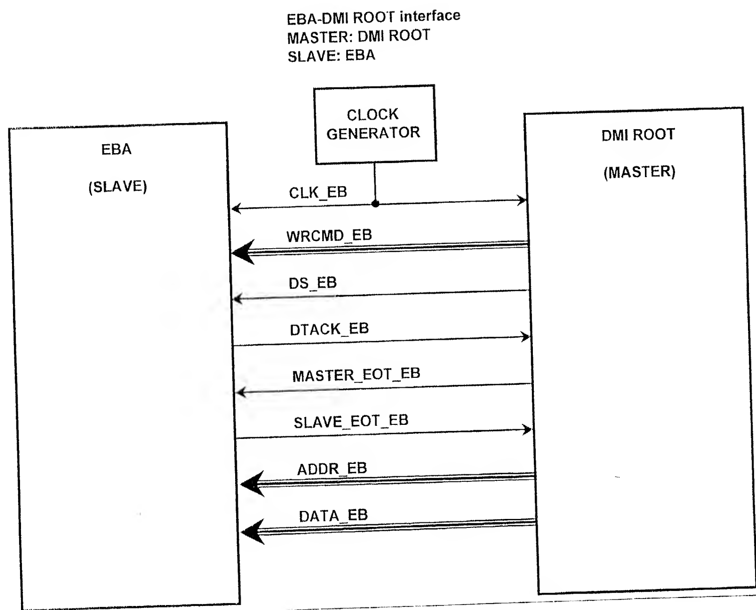
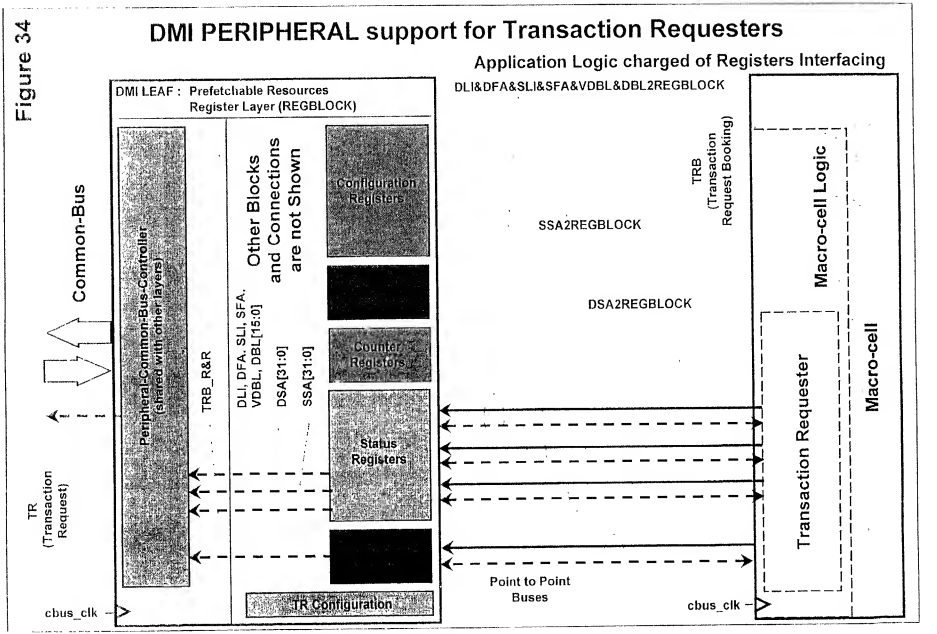


Figure 33

Prior Art

Figure 34


DMI PERIPHERAL support for Transaction Requesters
Application Logic charged of Registers Interfacing
DMI LEAF : Prefetchable Resources
Register Layer (REGBLOCK)
DLI&DFA&SLI&SFA&VDBL&DBL2REGBLOCK
Common-Bus
Peripheral-Common-Bus-Controller (shared with other layers)
TRB_R&R
DLI, DFA, SLI, SFA, VDBL, DBL[15:0]
DSA[31:0]
SSA[31:0]
Other Blocks and Connections are not Shown
Configuration Registers
Counter Registers
Status Registers
TR Configuration
TR (Transaction Request)
cbus_clk
SSA2REGBLOCK
DSA2REGBLOCK
TRB (Transaction Request Booking)
Point to Point Buses
Macro-cell Logic
Transaction Requester
Macro-cell
cbus_clk

20602O" OESTE9OOT

Figure 35

DMI Slave Mode Overall Algorithm Representation

Read Transaction from DMI PERIPHERAL + Read Transaction from EXTERNAL BUS AGENT

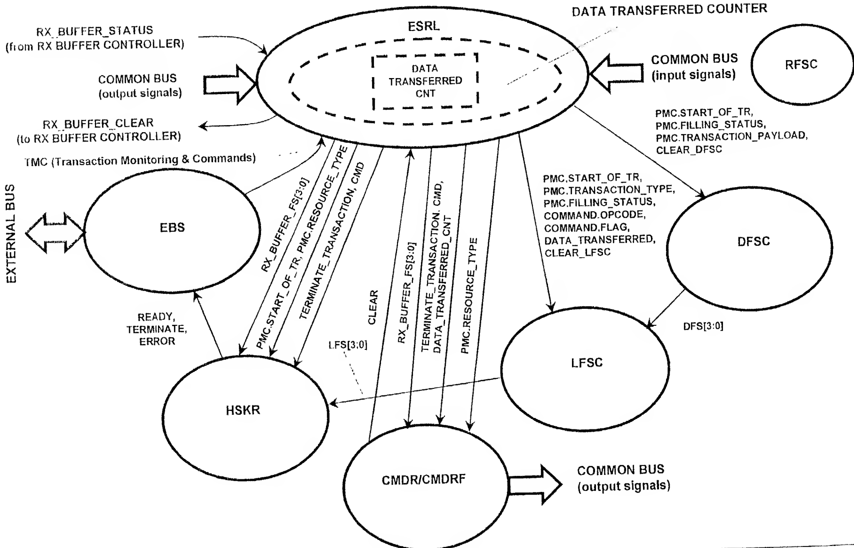


Figure 36

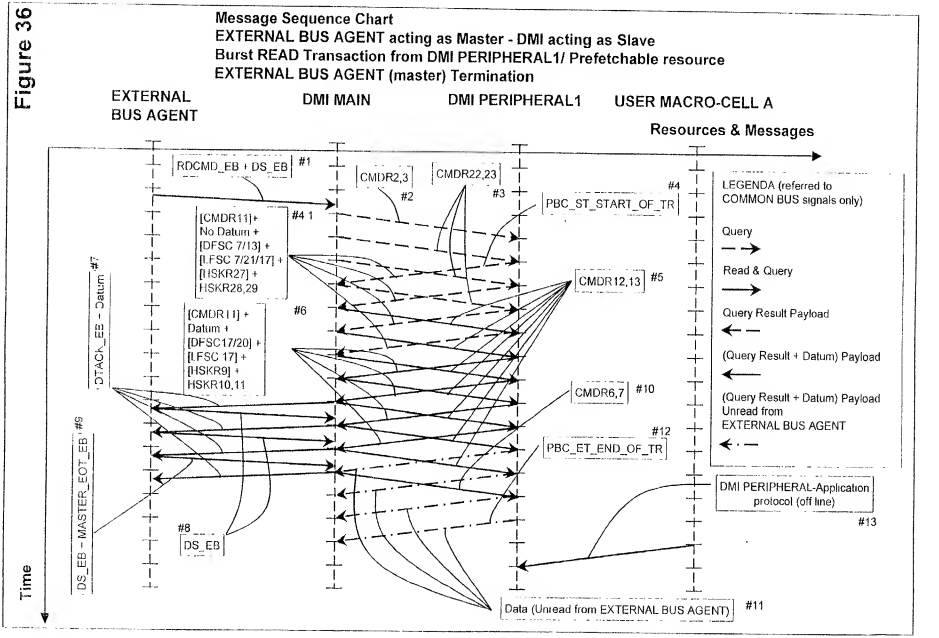

Message Sequence Chart
EXTERNAL BUS AGENT acting as Master - DMI acting as Slave
Burst READ Transaction from DMI PERIPHERAL1/ Prefetchable resource
EXTERNAL BUS AGENT (master) Termination
EXTERNAL BUS AGENT
DMI MAIN
DMI PERIPHERAL1
USER MACRO-CELL A
Resources & Messages
Time
RDCMD_EB + DS_EB
#1
CMDR2,3
CMDR22,23
#2
#3
#4
PBC_ST_START_OF_TR
[CMDR11] +
No Datum +
[DFSC 7/13] +
[LFSC 7/21/17] +
[HSKR27] +
HSKR28,29
#4 1
CMDR12,13
#5
[CMDR11] +
Datum +
[DFSC17/20] +
[LFSC 17] +
[HSKR9] +
HSKR10,11
#6
DTACK_EB + Datum
#7
CMDR6,7
#10
#12
PBC_ET_END_OF_TR
DS_EB + MASTER_EOT_EB
#9
#8
DS_EB
Data (Unread from EXTERNAL BUS AGENT)
#11
DMI PERIPHERAL-Application protocol (off line)
#13
LEGENDA (referred to COMMON BUS signals only)
Query
Read & Query
Query Result Payload
(Query Result + Datum) Payload
(Query Result + Datum) Payload Unread from EXTERNAL BUS AGENT

Figure 37

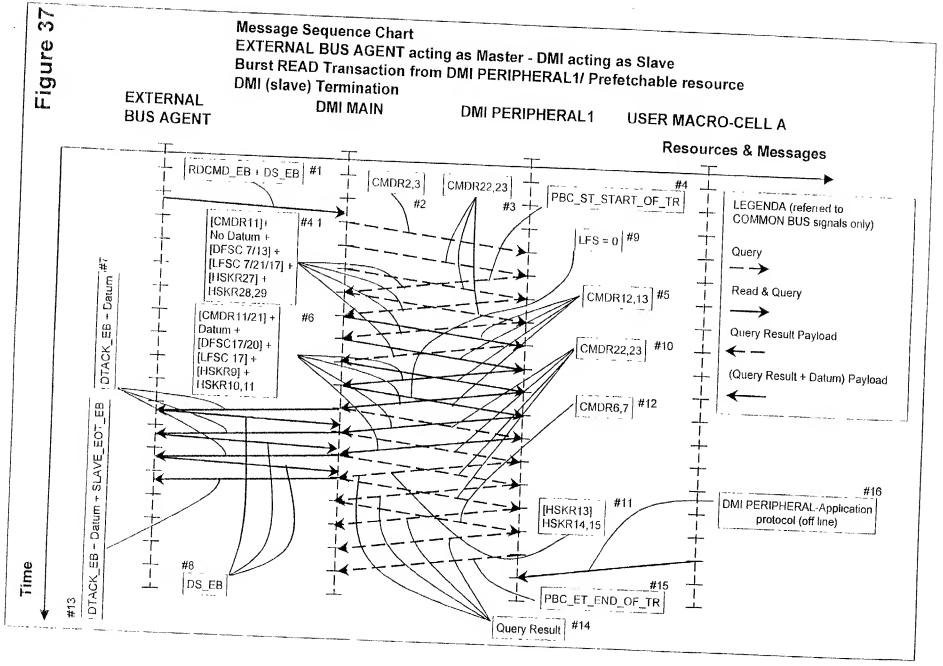
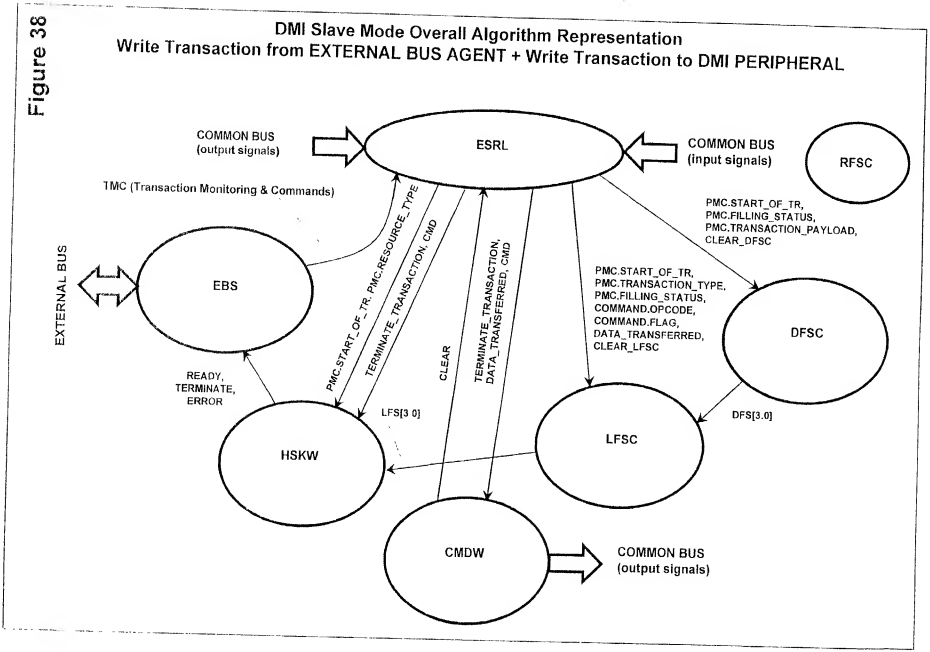


Figure 38



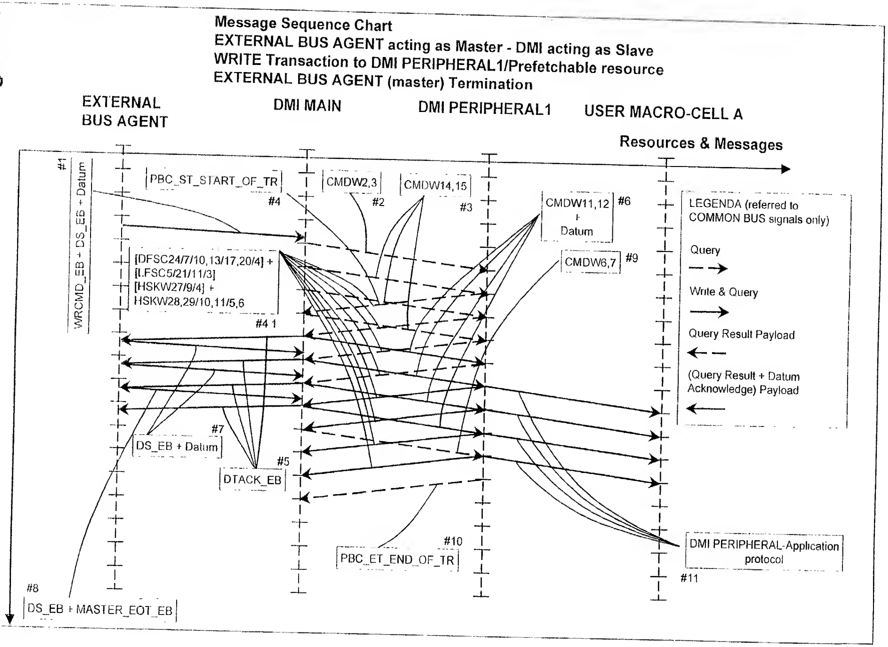

Message Sequence Chart
EXTERNAL BUS AGENT acting as Master - DMI acting as Slave
WRITE Transaction to DMI PERIPHERAL1/Prefetchable resource
EXTERNAL BUS AGENT (master) Termination
EXTERNAL BUS AGENT
DMI MAIN
DMI PERIPHERAL1
USER MACRO-CELL A
Resources & Messages
Time
#1
WRCMD_EB + DS_EB + Datum
PBC_ST_START_OF_TR
#4
CMDW2,3
#2
CMDW14,15
#3
CMDW11,12 + Datum
#6
CMDW6,7
#9
[DFSC24/7/10,13/17,20/4] +
[LFSC5/21/11/3]
[HSKW27/9/4] +
HSKW28,29/10,11/5,6
#4 1
DS_EB + Datum
#7
DTACK_EB
#5
PBC_ET_END_OF_TR
#10
DMI PERIPHERAL-Application protocol
#11
#8
DS_EB + MASTER_EOT_EB
LEGENDA (referred to COMMON BUS signals only)
Query
Write & Query
Query Result Payload
(Query Result + Datum Acknowledge) Payload

Figure 39

Figure 40

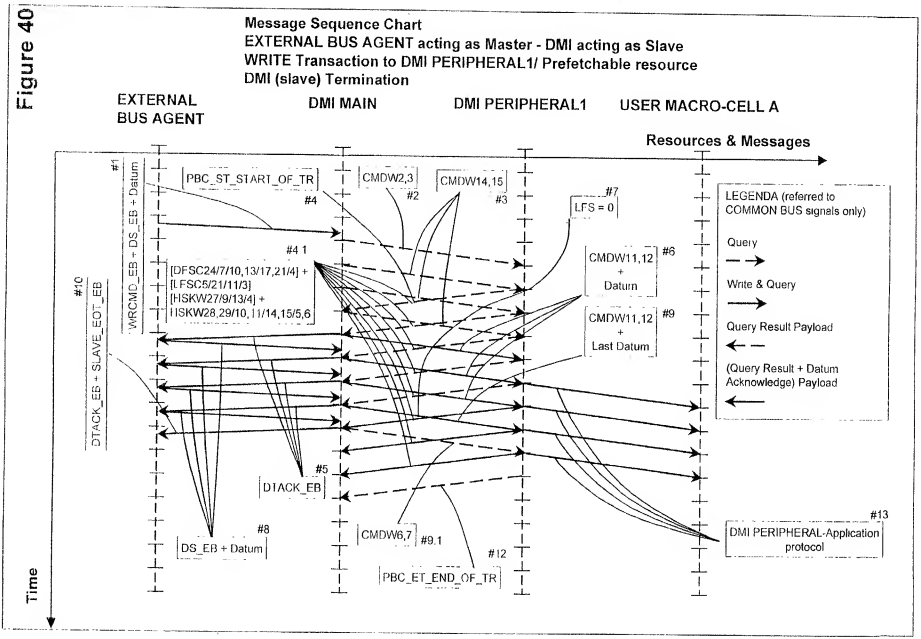
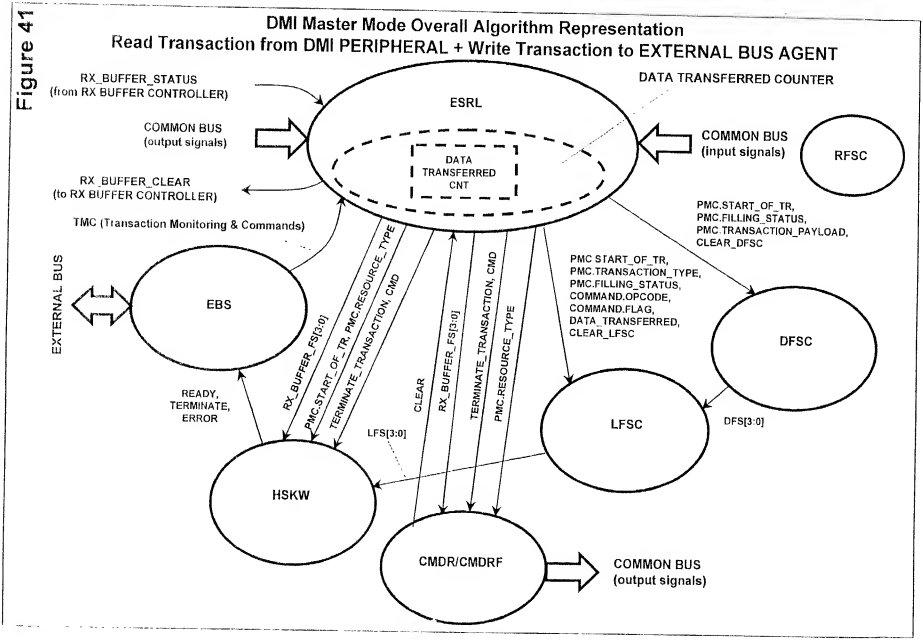


Figure 41



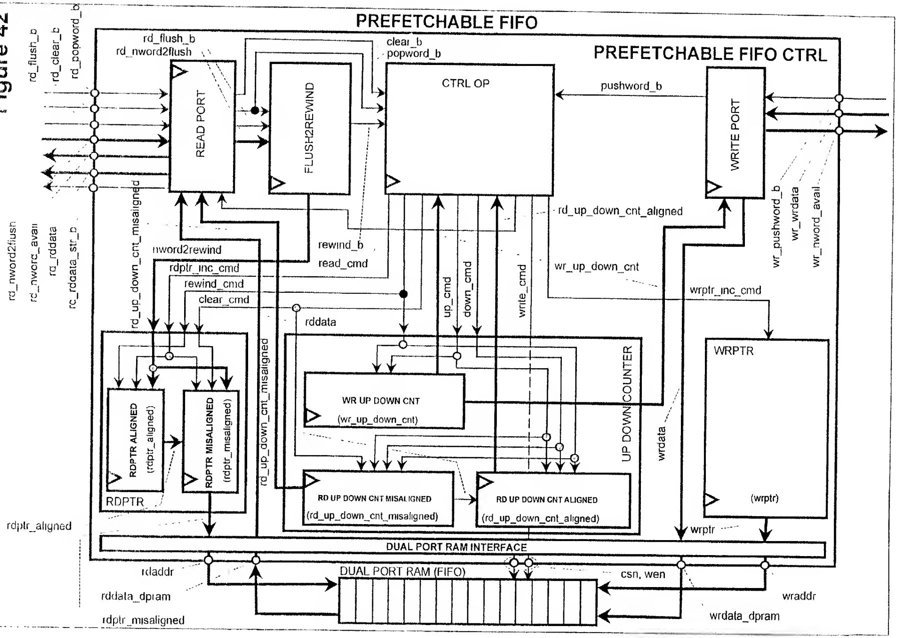
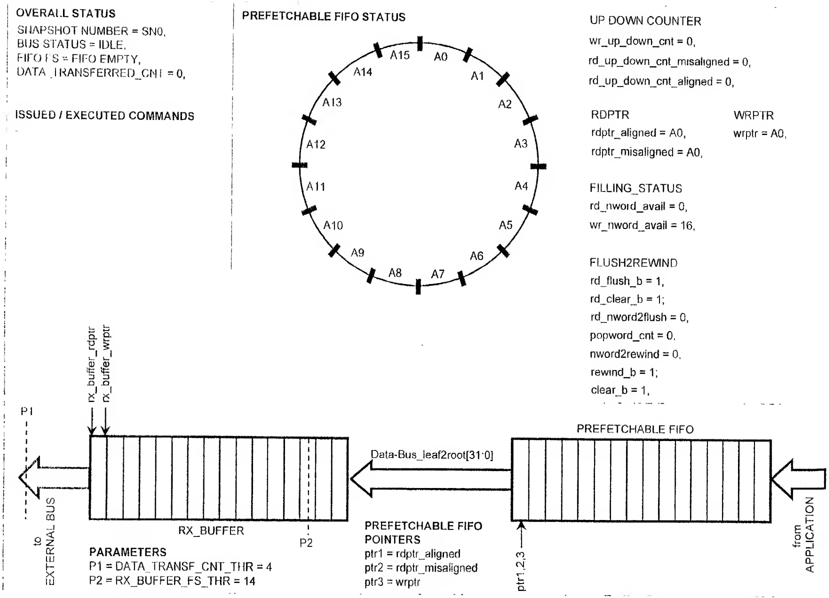

PREFETCHABLE FIFO
PREFETCHABLE FIFO CTRL
rd_flush_b
rd_clear_b
rd_popword_b
rd_nword2flush
rd_nword_avail
rd_rddata
rd_rddata_str_b
rd_flush_b
rd_nword2flush
READ PORT
FLUSH2REWIND
clear_b
popword_b
CTRL OP
pushword_b
WRITE PORT
wr_pushword_b
wr_wrdata
wr_nword_avail
rd_up_down_cnt_aligned
rd_up_down_cnt_misaligned
nword2rewind
rdptr_inc_cmd
rewind_cmd
clear_cmd
rewind_b
read_cmd
rddata
up_cmd
down_cmd
write_cmd
wr_up_down_cnt
wrptr_inc_cmd
RDPTR ALIGNED
(rdptr_aligned)
RDPTR MISALIGNED
(rdptr_misaligned)
RDPTR
rd_up_down_cnt_misaligned
WR UP DOWN CNT
(wr_up_down_cnt)
UP DOWN COUNTER
RD UP DOWN CNT MISALIGNED
(rd_up_down_cnt_misaligned)
RD UP DOWN CNT ALIGNED
(rd_up_down_cnt_aligned)
wrdata
WRPTR
(wrptr)
wrptr
rdptr_aligned
DUAL PORT RAM INTERFACE
rdaddr
DUAL PORT RAM (FIFO)
csn, wen
rddata_dpram
rdptr_misaligned
wraddr
wrdata_dpram

Figure 42

Figure 43


OVERALL STATUS
SNAPSHOT NUMBER = SN0,
BUS STATUS = IDLE,
FIFO FS = FIFO EMPTY,
DATA_TRANSFERRED_CNT = 0,
ISSUED / EXECUTED COMMANDS
PREFETCHABLE FIFO STATUS
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
UP DOWN COUNTER
wr_up_down_cnt = 0,
rd_up_down_cnt_misaligned = 0,
rd_up_down_cnt_aligned = 0,
RDPTR
rdptr_aligned = A0,
rdptr_misaligned = A0,
WRPTR
wrptr = A0,
FILLING_STATUS
rd_nword_avail = 0,
wr_nword_avail = 16,
FLUSH2REWIND
rd_flush_b = 1,
rd_clear_b = 1;
rd_nword2flush = 0,
popword_cnt = 0,
nword2rewind = 0,
rewind_b = 1;
clear_b = 1,
P1
rx_buffer_rdptr
rx_buffer_wrptr
to EXTERNAL BUS
RX_BUFFER
P2
PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14
Data-Bus_leaf2root[31:0]
PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr
ptr1,2,3
PREFETCHABLE FIFO
from APPLICATION

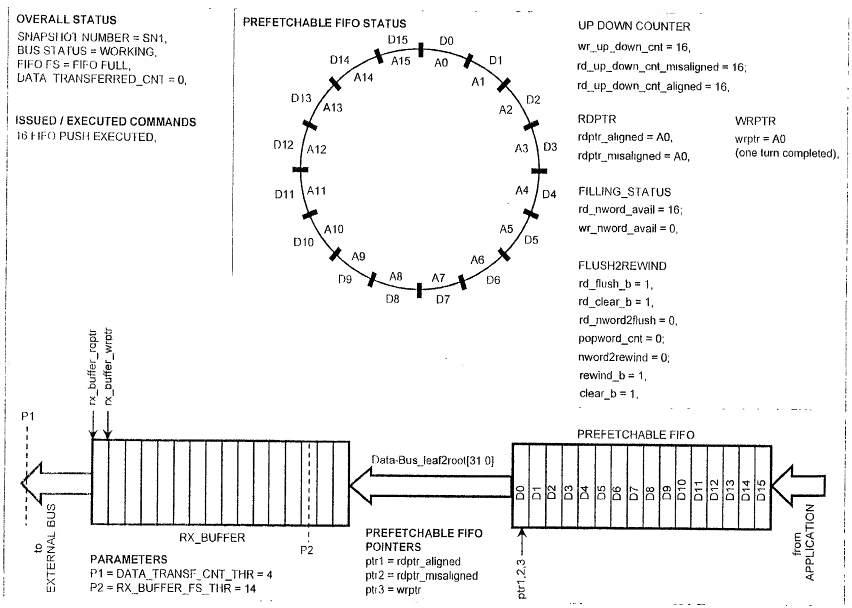

OVERALL STATUS
SNAPSHOT NUMBER = SN1,
BUS STATUS = WORKING,
FIFO FS = FIFO FULL,
DATA TRANSFERRED_CNT = 0,
ISSUED / EXECUTED COMMANDS
16 FIFO PUSH EXECUTED,
PREFETCHABLE FIFO STATUS
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
UP DOWN COUNTER
wr_up_down_cnt = 16,
rd_up_down_cnt_misaligned = 16;
rd_up_down_cnt_aligned = 16,
RDPTR
rdptr_aligned = A0,
rdptr_misaligned = A0,
WRPTR
wrptr = A0
(one turn completed),
FILLING_STATUS
rd_nword_avail = 16;
wr_nword_avail = 0,
FLUSH2REWIND
rd_flush_b = 1,
rd_clear_b = 1,
rd_nword2flush = 0,
popword_cnt = 0;
nword2rewind = 0;
rewind_b = 1,
clear_b = 1,
P1
rx_buffer_rdptr
rx_buffer_wrptr
to EXTERNAL BUS
RX_BUFFER
P2
PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14
Data-Bus_leaf2root[31 0]
PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr
ptr1,2,3
PREFETCHABLE FIFO
from APPLICATION

Figure 44

Figure 45

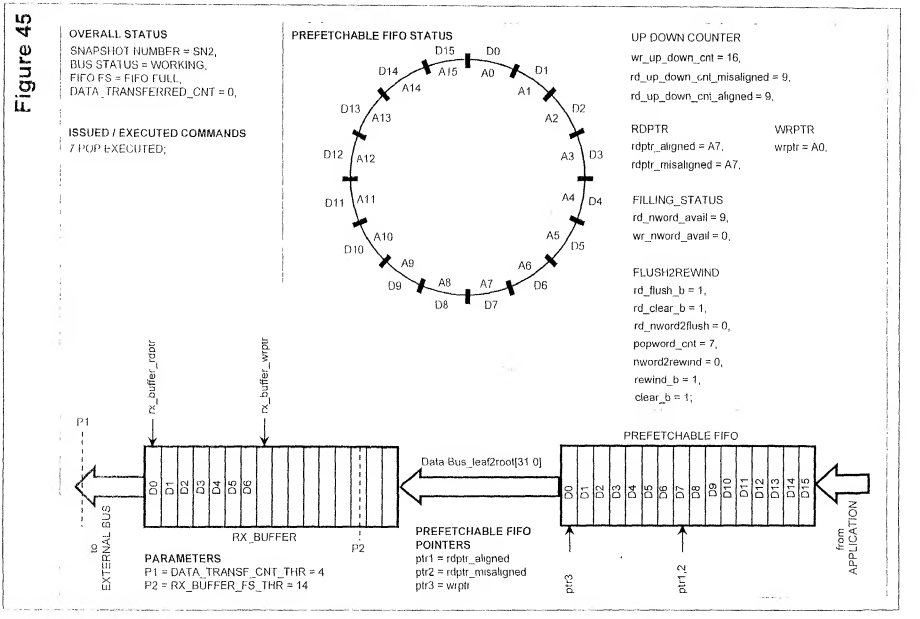

OVERALL STATUS
SNAPSHOT NUMBER = SN2,
BUS STATUS = WORKING,
FIFO FS = FIFO FULL,
DATA_TRANSFERRED_CNT = 0,
ISSUED / EXECUTED COMMANDS
7 POP EXECUTED;
PREFETCHABLE FIFO STATUS
D15 D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14
A15 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14
UP DOWN COUNTER
wr_up_down_cnt = 16,
rd_up_down_cnt_misaligned = 9,
rd_up_down_cnt_aligned = 9,
RDPTR
rdptr_aligned = A7,
rdptr_misaligned = A7,
WRPTR
wrptr = A0,
FILLING_STATUS
rd_nword_avail = 9,
wr_nword_avail = 0,
FLUSH2REWIND
rd_flush_b = 1,
rd_clear_b = 1,
rd_nword2flush = 0,
popword_cnt = 7,
nword2rewind = 0,
rewind_b = 1,
clear_b = 1;
rx_buffer_rdptr
rx_buffer_wrptr
P1
D0 D1 D2 D3 D4 D5 D6
RX_BUFFER
P2
to EXTERNAL BUS
PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14
Data Bus_leaf2root[31 0]
PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr
PREFETCHABLE FIFO
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
ptr3
ptr1,2
from APPLICATION

Figure 46

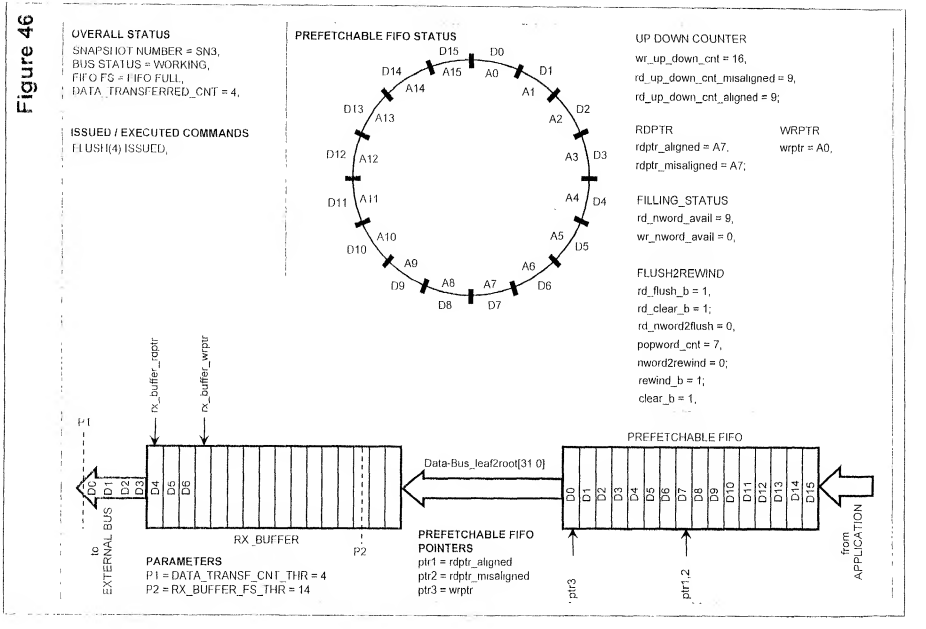

OVERALL STATUS
SNAPSHOT NUMBER = SN3,
BUS STATUS = WORKING,
FIFO FS = FIFO FULL,
DATA_TRANSFERRED_CNT = 4,
ISSUED / EXECUTED COMMANDS
FLUSH(4) ISSUED,
PREFETCHABLE FIFO STATUS
D15 D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14
A15 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14
UP DOWN COUNTER
wr_up_down_cnt = 16,
rd_up_down_cnt_misaligned = 9,
rd_up_down_cnt_aligned = 9;
RDPTR
rdptr_aligned = A7,
rdptr_misaligned = A7;
WRPTR
wrptr = A0,
FILLING_STATUS
rd_nword_avail = 9,
wr_nword_avail = 0,
FLUSH2REWIND
rd_flush_b = 1,
rd_clear_b = 1;
rd_nword2flush = 0,
popword_cnt = 7,
nword2rewind = 0;
rewind_b = 1;
clear_b = 1,
rx_buffer_rdptr
rx_buffer_wrptr
P1
D0 D1 D2 D3 D4 D5 D6
RX_BUFFER
P2
to EXTERNAL BUS
PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14
Data-Bus_leaf2root[31:0]
PREFETCHABLE FIFO
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr
ptr3
ptr1,2
from APPLICATION

Figure 47

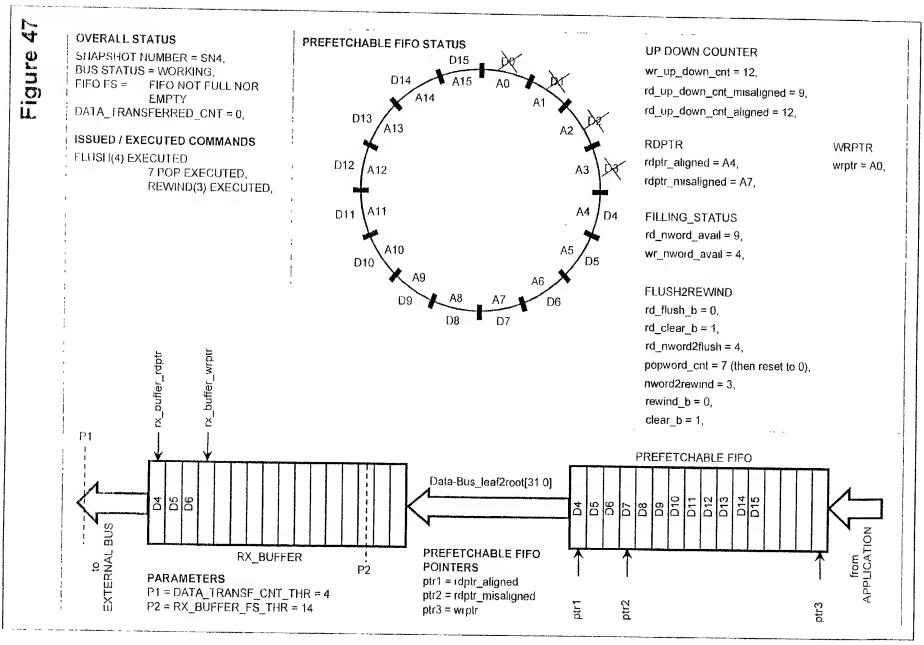


Figure 48

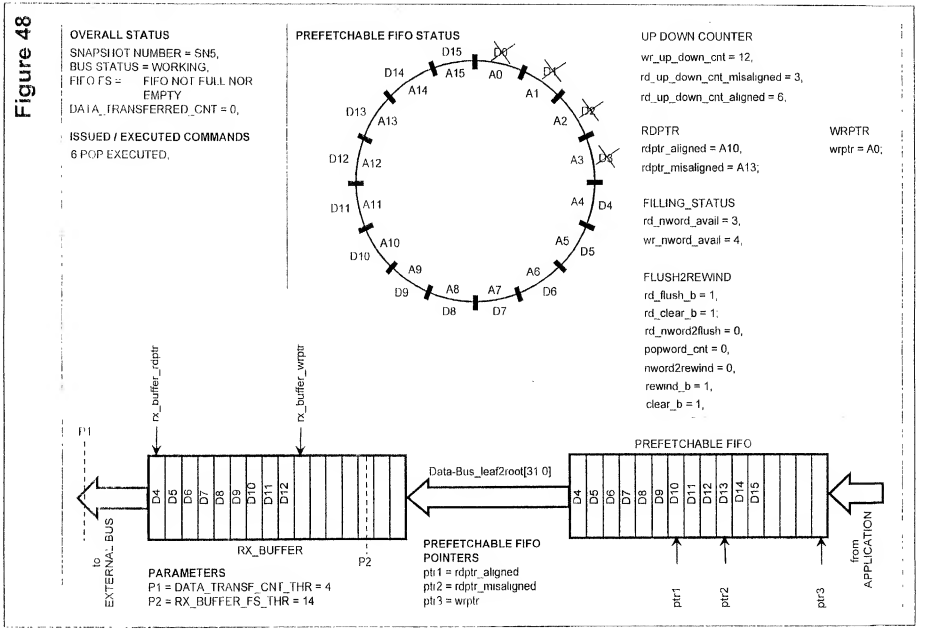
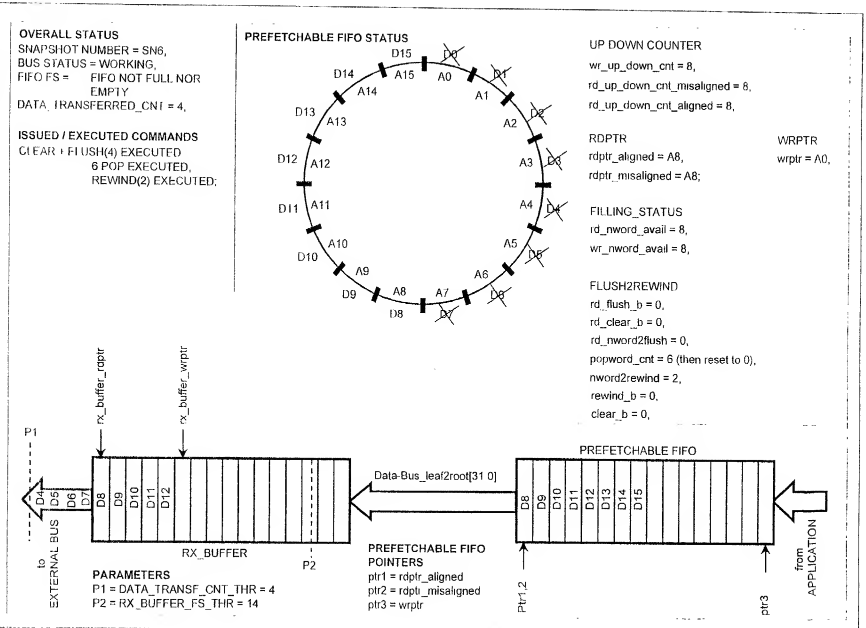


Figure 49


OVERALL STATUS
SNAPSHOT NUMBER = SN6,
BUS STATUS = WORKING,
FIFO FS = FIFO NOT FULL NOR EMPTY
DATA_TRANSFERRED_CNT = 4,
ISSUED / EXECUTED COMMANDS
CLEAR + FLUSH(4) EXECUTED
6 POP EXECUTED,
REWIND(2) EXECUTED;
PREFETCHABLE FIFO STATUS
D15
D0
A15
A0
D14
D1
A14
A1
D13
A13
D2
A2
D12
A12
A3
D3
D11
A11
A4
D4
A10
A5
D10
D5
A9
A6
D9
A8
A7
D6
D8
D7
UP DOWN COUNTER
wr_up_down_cnt = 8,
rd_up_down_cnt_misaligned = 8,
rd_up_down_cnt_aligned = 8,
RDPTR
rdptr_aligned = A8,
rdptr_misaligned = A8;
WRPTR
wrptr = A0,
FILLING_STATUS
rd_nword_avail = 8,
wr_nword_avail = 8,
FLUSH2REWIND
rd_flush_b = 0,
rd_clear_b = 0,
rd_nword2flush = 0,
popword_cnt = 6 (then reset to 0),
nword2rewind = 2,
rewind_b = 0,
clear_b = 0,
P1
rx_buffer_rdptr
rx_buffer_wrptr
D4
D5
D6
D7
D8
D9
D10
D11
D12
to
EXTERNAL BUS
RX_BUFFER
P2
PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14
Data-Bus_leaf2root[31 0]
PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr
PREFETCHABLE FIFO
D8
D9
D10
D11
D12
D13
D14
D15
Ptr1,2
ptr3
from
APPLICATION

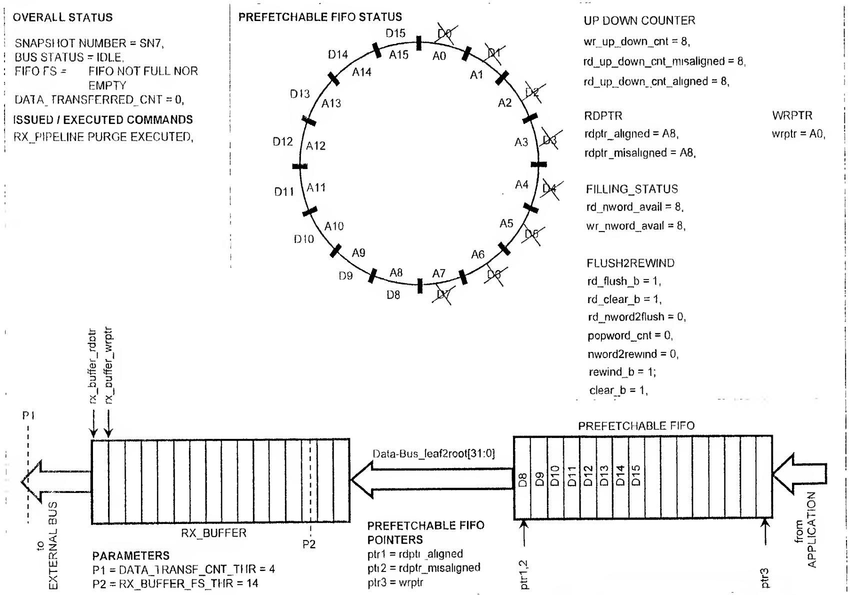

OVERALL STATUS
SNAPSHOT NUMBER = SN7,
BUS STATUS = IDLE,
FIFO FS = FIFO NOT FULL NOR EMPTY
DATA_TRANSFERRED_CNT = 0,
ISSUED / EXECUTED COMMANDS
RX_PIPELINE PURGE EXECUTED,
PREFETCHABLE FIFO STATUS
D15 A15 A0 D0 A1 D1 A2 D2 A3 D3 A4 D4 A5 D5 A6 D6 A7 D7 A8 D8 A9 D9 A10 D10 A11 D11 A12 D12 A13 D13 A14 D14
UP DOWN COUNTER
wr_up_down_cnt = 8,
rd_up_down_cnt_misaligned = 8,
rd_up_down_cnt_aligned = 8,
RDPTR
rdptr_aligned = A8,
rdptr_misaligned = A8,
WRPTR
wrptr = A0,
FILLING_STATUS
rd_nword_avail = 8,
wr_nword_avail = 8,
FLUSH2REWIND
rd_flush_b = 1,
rd_clear_b = 1,
rd_nword2flush = 0,
popword_cnt = 0,
nword2rewind = 0,
rewind_b = 1;
clear_b = 1,
P1
rx_buffer_rdptr
rx_buffer_wrptr
to EXTERNAL BUS
RX_BUFFER
P2
PARAMETERS
P1 = DATA_TRANSF_CNT_THR = 4
P2 = RX_BUFFER_FS_THR = 14
Data-Bus_leaf2root[31:0]
PREFETCHABLE FIFO POINTERS
ptr1 = rdptr_aligned
ptr2 = rdptr_misaligned
ptr3 = wrptr
PREFETCHABLE FIFO
D8 D9 D10 D11 D12 D13 D14 D15
ptr1,2
ptr3
from APPLICATION

Figure 50

Figure 51

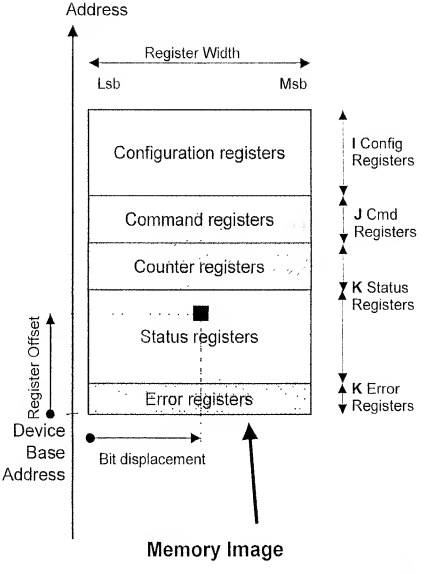


Figure 52

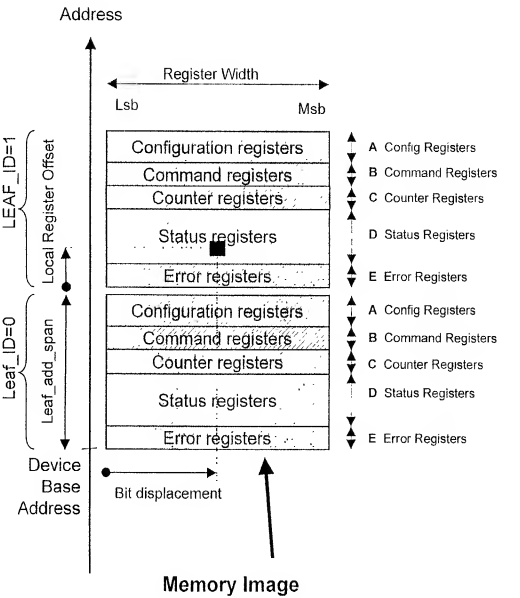


Figure 53

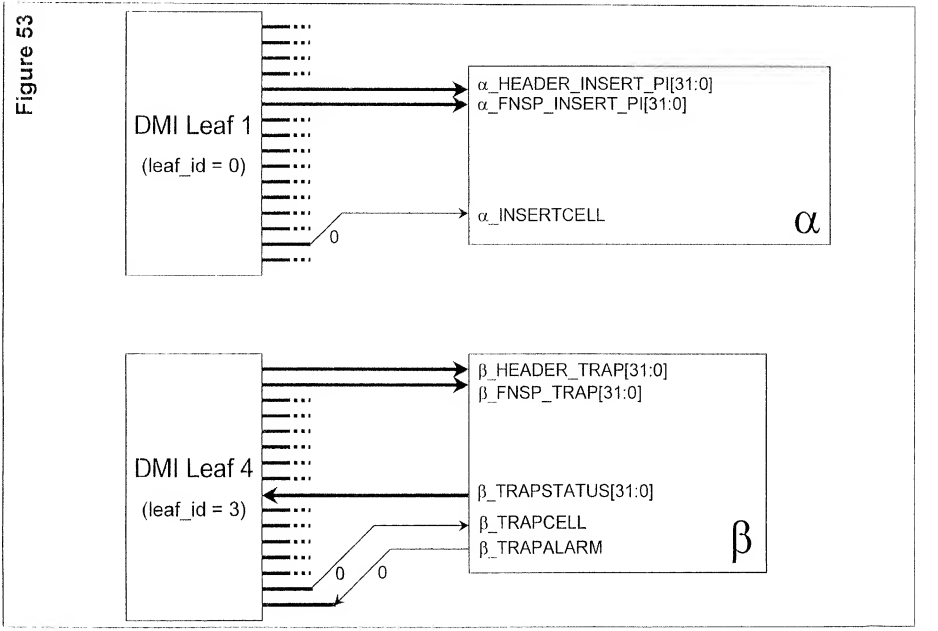


Figure 54

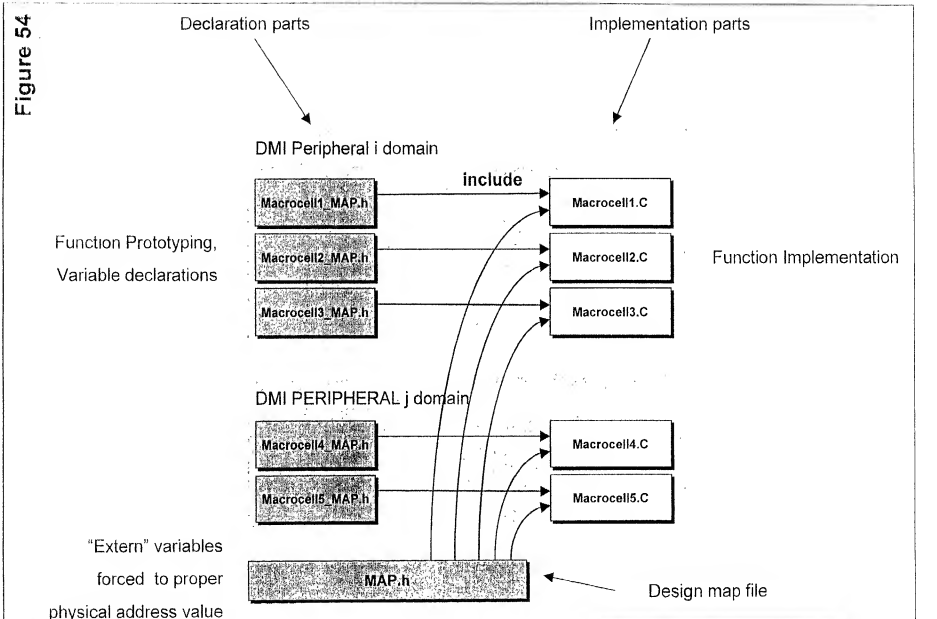
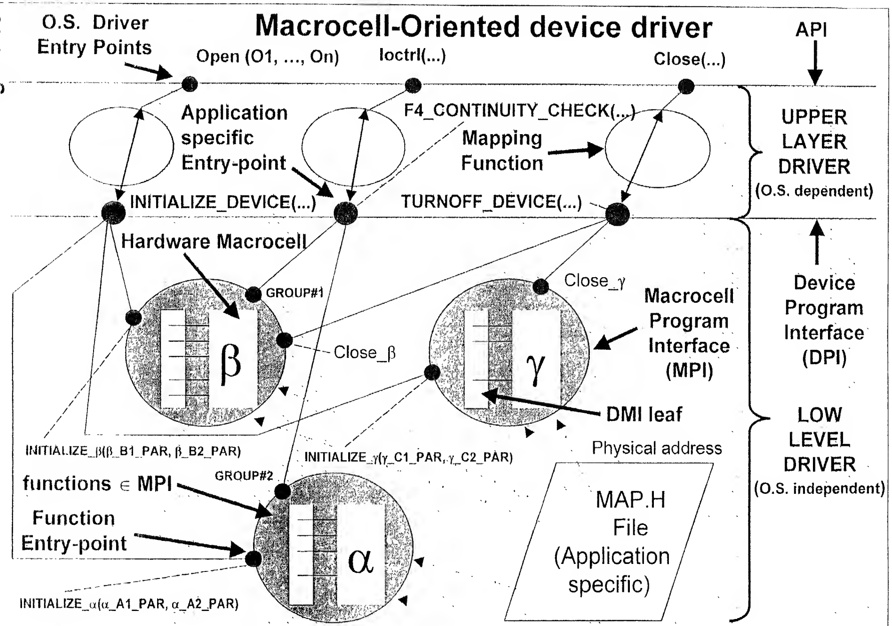


Figure 55



Macrocell-Oriented device driver
O.S. Driver
Entry Points
Open (O1, ..., On)
Ioctrl(...)
Close(...)
API
Application
specific
Entry-point
F4_CONTINUITY_CHECK(...)
Mapping
Function
INITIALIZE_DEVICE(...)
TURNOFF_DEVICE(...)
UPPER
LAYER
DRIVER
(O.S. dependent)
Hardware Macrocell
GROUP#1
Close_β
β
Close_γ
γ
Macrocell
Program
Interface
(MPI)
Device
Program
Interface
(DPI)
DMI leaf
LOW
LEVEL
DRIVER
(O.S. independent)
Physical address
INITIALIZE_β(β_B1_PAR, β_B2_PAR)
INITIALIZE_γ(γ_C1_PAR, γ_C2_PAR)
GROUP#2
functions ∈ MPI
Function
Entry-point
α
MAP.H
File
(Application
specific)
INITIALIZE_α(α_A1_PAR, α_A2_PAR)